History of SCOPES

- 1st workshop: Schloss Dagstuhl, Wadern (Germany), Aug. 31st to Sept. 2nd, 1994, P. Marwedel, G. Goossens
- 2nd workshop: IMEC, Leuven (Belgium), March 18-20, 1996, G. Goossens, P. Marwedel
- 3rd workshop: Haus Bommerholz, Witten (Germany), March 4-6, 1998, P. Marwedel, R. Leupers
- 4th workshop: Schloss Rheinfels, St. Goar (Germany), Sept. 1-3, 1999, P. Marwedel, S. Bashford, R. Leupers
- 5th workshop: Schloss Rheinfels, St. Goar (Germany), March 20-22, 2001, P. Marwedel, S. Steinke, R. Leupers
- 6th workshop: joint LCTES/SCOPES workshop at Berlin, June 19-21, 2002, S. Devadas, P. Marwedel
- 7th workshop: TU Wien, Sept. 24th-26th, 2003, A. Krall
- 8th workshop: Amsterdam /London

Publications

- 1st workshop: P. Marwedel, G. Goossens: Code Generation for Embedded Processors, Kluwer, 1995
- 2nd workshop: handouts
- 3rd workshop: special issue of Design Automation of Embedded Systems, **4**, 1999
- 4th workshop: special issue of TODAES, Volume 5 Number 4, 2000
- 5th: IEEE TCAD, late 2001/early 2002
- 6th: ACM SIGPLAN Notices
- 7th: Springer LNCS

What's special about SCOPES ?

- Focussed
- Good mix of industrial and academic participants
- Emphasis on recent results
- Complements traditional conferences
- Impact on scope of conferences
- Participants from groups working actively in the field
- Interactive atmosphere

Current trends

1. Optimizations for embedded processors (resource awareness)
   - Register Allocation for heterogenous register files
   - Code compaction with predicated instructions
   - Exploitation of Dual Instruction sets
   - Graph-based code selection
   - Exploitation of SIMD/PACK instructions
   - Recursion removal
   - Exploitation of zero overhead loop buffer
   - Memory and cache optimizations
   - Extraction of architectural parameters
2. Retargetability
   - Reconstruction of control flow for retargetable optim.
   - Extraction of instruction schedulers.

Future directions?

More optimizations:

- For VLIW ?
- For energy ?
- For avoiding the memory wall?
- Early optimizations
- Include DVS?
- Optimizing the worst case timing?
- Network processors
- Verified code?

Can optimization techniques cope with increasing requirements?