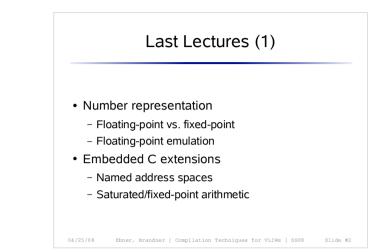
## VU2 185.324

Compilation Techniques for VLIW Architectures

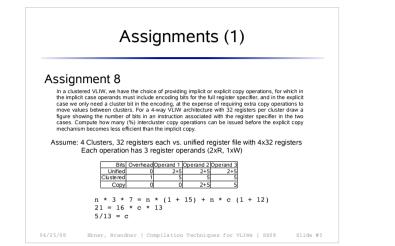
Dietmar Ebner ebner@complang.tuwien.ac.at Florian Brandner brandner@complang.tuwien.ac.at

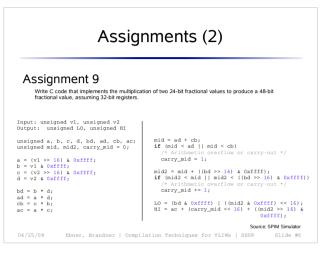
http://complang.tuwien.ac.at/cd/vliw

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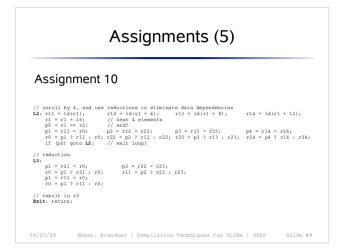


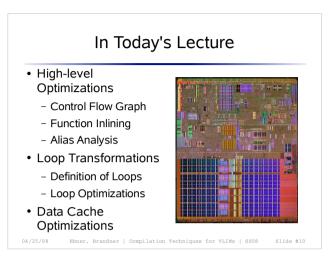


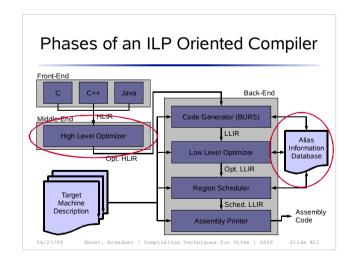


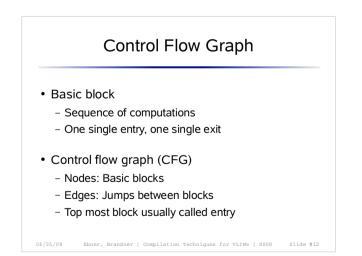
Assignments (3)	
	ified register file with 32-bit registers (r0-r31), and
registers (p0-p7), and according comparison opera using load/store operations (ld, st). The archit select instruction. There are no restrictions on the	· · · · · · · · · · · · · · · · · · ·
	foo: r0 = UINT_MAX; p0 = r2 == 0;

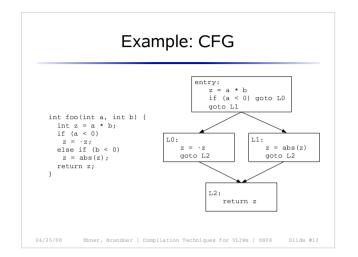
Assignments (4) Assignment 10 – Unrolling with pre-conditioning, reductions and ILP		
<pre>// pre-conditioning L0: r3 = 1d(r1); r1 = r1 + 4; r10 = r10 - 1; p1 = r10 != 0; nop // wait for load p1 = r3 &lt; r0; if (p1) goto L0; r0 = p1 ? r3 : r0;</pre>		
<pre>// prepare for unrolled loop L1: p0 = r2 == 0;</pre>		
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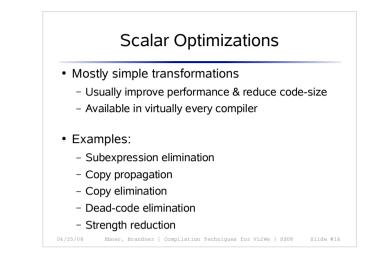


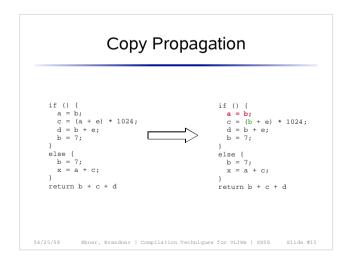


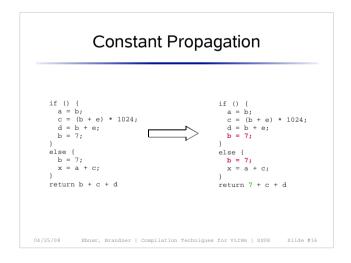


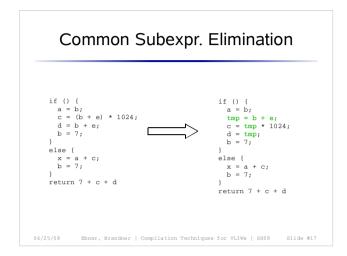


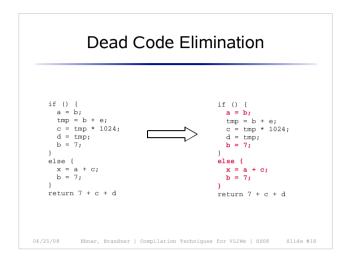


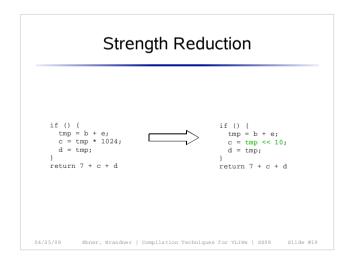


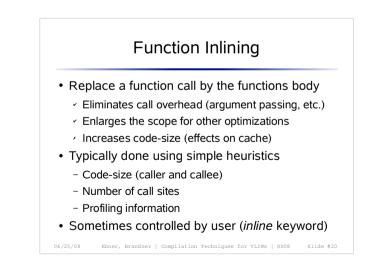


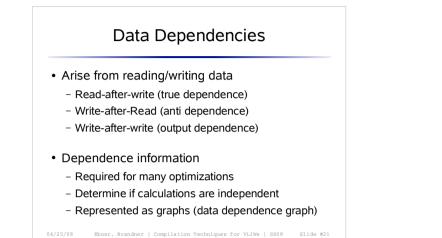


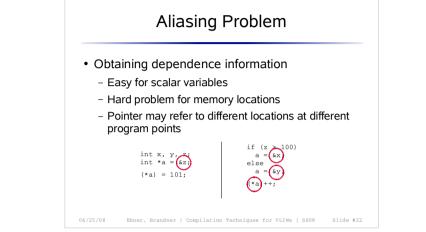
















- Flow-insensitive AA
  - Alias information independent of program locations
- Flow-sensitive AA
  - Alias information for each program point
  - More precise & more complex
- May vs. must aliasing
  - Determine if a pointer is guaranteed to refer to a particular memory location

